Abstracts

A 5-Gb/s Decision Circuit Fabricated in a 1.5-µm Super-Self-Aligned Silicon Bipolar IC Technology

R.G. Swartz, V.D. Archer, T.Y. Chiu, Y. Ota, A.M. Voshchenkov, T. Long, K. Moerschel and W. Possanza. "A 5-Gb/s Decision Circuit Fabricated in a 1.5-µm Super-Self-Aligned Silicon Bipolar IC Technology." 1991 Microwave and Guided Wave Letters 1.5 (May 1991 [MGWL]): 103-106.

The design and, experimental measurements on a clocked decision circuit for optical communication applications are reviewed. The circuit, fabricated in a 1.5-µm super-selfaligned silicon bipolar technology, yields a BER <10/sup -9/ at a bit rate of 5 Gb/s. At 2.5 Gb/s, the small signal input data sensitivity is 10 mV, the clock timing margin is 320 ps (288°), the output eye opening is 300 ps (270°), and the rise/fall times are about 100 ps.

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